Design and Implementation of an Electronic Device for Three-Phase Sinusoidal Signal Generator with Harmonic Injection Using Hardware Description Language

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Abstract— **This work focuses on designing and implementing a three-phase sinusoidal signal generator that can inject harmonics of different orders, using an FPGA as the core hardware component. We will analyze how these signals affect the performance of a synchronous reluctance motor under different load conditions. The ultimate goal is to integrate this generator into a complete controller for three-phase reluctance motors. The project aims to improve the quality of the current signal and reduce torque ripple, which are common challenges in controlling these types of motors. The generator provided the signal composed of the desired harmonics, allowing visualization of the signal across different operating frequencies.**

Keywords— Signal Generator, Harmonics, FPGA, Reluctance Motor, Torque Ripple.

I. Introduction

We are experiencing a transitional phase in mobility, where electric vehicles are increasingly gaining ground, driven by governmental and global policies and targets aimed at reducing greenhouse gas emissions, as well as their growing popularity due to technological advancements and lower maintenance costs compared to combustion vehicles [1]. This transition is further accelerated by the use of lithium batteries, which provide greater autonomy and applicability. Simultaneously, significant transformations are occurring in our energy matrix, with renewable and clean sources such as wind and solar energy becoming more prevalent[2].

Significant and disruptive advances, such as artificial intelligence, communication mechanisms, 5G technology, cryptocurrencies, and blockchain, are becoming integral parts of our daily lives. Humanity evolves and overcomes challenges, whether it be instant communication, generating clean and sustainable energy, or democratizing access to technology and information, all accessible from the screen of our smartphones.

It is within this context of innovation, technology, and overcoming challenges that this work is inspired. The premise is to reduce the consumption of rare earth magnets for electric mobility applications and to use resources like artificial intelligence and machine learning to ensure that the latest initiatives and advancements in digital control project development—via software programming and practical hardware implementation—work in conjunction with innovative designs of reluctance electric motors, performing efficiently, with low energy consumption, power dissipation, and harmonic content [1], [2], [3].

II. Bibliographic Review

Given the above scenario, this research focuses on developing a sinusoidal signal generator on an FPGA to power and control a synchronous reluctance motor (SynRM), used by most electric vehicle manufacturers in their commercial models. Different harmonics will be injected into the fundamental three-phase supply signal to mitigate harmonic distortions generated primarily by its construction and operation [3], [4], [5].

The synchronous reluctance motor consists of a conventional three-phase wound stator, similar to an induction motor, and a rotor made of ferromagnetic material. The variation in its reluctance results in motion, as the rotor tends to move to align its poles in a position of minimum reluctance relative to the poles established by the stator, thus developing torque based on the magnetic reluctance variation of its geometry [3]. Figure 1 illustrates the main types of rotors in reluctance motors:
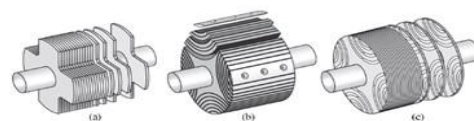

Fig. 1. Different types of rotors used in SyRM: (a) Simple salient pole rotor; (b) Axially laminated rotor; (c) Transversely laminated rotor [3]

The main advantages of using this type of motor, besides avoiding the use of materials like rare earth magnets, which entail high costs due to their extraction and manufacturing processes, and considering their limited availability, include their low cost, high efficiency, operation at low temperatures, simple and robust structure. However, there are also areas for improvement such as power factor, operation at high speeds, and torque ripple [6].

As the focus of this research, we will primarily examine torque ripple, typically caused by the interaction between the spatial harmonics of the electrical load and the anisotropic geometry of the rotor and its interaction with the stator. In addition to developing and implementing a signal generator in FPGA for controlling reluctance motors via PWM, we can inject harmonics of orders that are most relevant in an attempt to nullify these noises, identified through FFT (Fast Fourier Transformation), and improve efficiency and performance during operation [4], [7].Control signals for the reluctance motor will be generated using the Intel Cyclone IV E FPGA with a 60nm processor, specifically on the DE2-115 board. The generator will be programmed in VHDL and compiled using the Quartus Prime II software [8], [9].

The FPGA (Field-Programmable Gate Array) is an integrated circuit technology that enables the programming and implementation of digital circuits in hardware through programming languages like VHDL, Verilog, among others. In summary, FPGAs consist of blocks such as interface I/O, memory, processor, converters, logic units, among other resources. The DE2-115 board, commonly used for educational purposes, already includes some native features such as USB input for configuration and processor programming, a seven-segment display, push-button and slide-button with anti-debouncing system and protection diodes, external 50MHz clock, memories, VGA video output, a socket for GPIO connection, in addition to the Cyclone IV E FPGA with a 60nm processor, among others [8]. The board with its peripherals can be seen in Figure 2:

Fig. 2. DE2-115 board with indications of its peripherals

III. PROPOSED ARCHITECTURE

The basic architecture of the FPGA controller, developed in VHDL, will initially consist of a block responsible for generating the fundamental signal, which can vary from 50Hz to 1kHz, defined range to understand the behavior of harmonic generation in different operating modes of the SyRM, and other pre-established frequencies, namely the 6th, 12th, 18th, and 24th harmonics. The stator pole configuration and its interaction with the rotor's anisotropic geometry induce observable ripple, notably influencing noise distribution at the 6th-order harmonics [4]. These harmonics will be summed with the fundamental

signal and injected into the analyzed load. Additionally, there will be blocks for generating the sinusoids, attenuating the amplitude of the harmonics, summing them, and generating the output PWM signal [5], [7].

The Pulse Width Modulation (PWM) modulation technique used in the project to generate the sinusoidal signal at the generator output synthesizes a variable amplitude and frequency AC waveform from a DC bus, through the generation of a binary pulse train signal. The width of the generated pulses depends on the desired waveform at the output of the inverter block, which is typically composed of transistors in a bridge arrangement. Its application is highly effective in electric motor control as it allows for precise speed and torque control [7]. The desired signal type at the output of the signal generator developed in this project is a sine wave, with a frequency ranging from 50Hz to 1kHz, composed of four additional sinusoids, with frequencies corresponding to the predefined harmonics. This signal enters the PWM block of the signal generator structure and is sampled at a frequency adjusted based on the FPGA clock [5], [7].

IV. TESTS AND SOFTWARE APPLICATION

The project was initially developed in Quartus, where each block composing its architecture was designed in VHDL. Each function was developed and compiled, resulting in the creation of a block diagram showing the final circuit layout, as shown in Figure 3.
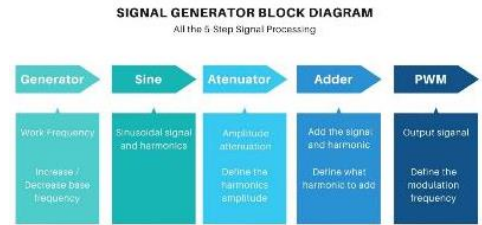

Fig. 3. Block diagram illustrating the signal generator implemented in Quartus, with each block individually labeled.

The 'Generator' block, depicted in Figure 4, is responsible for generating the operating frequency signals for the motor and its harmonics. Its input variables include the 50MHz FPGA clock, 'Reset' status, and commands for increasing or decreasing the motor's operating frequency, which can range from 50Hz to 1kHz.
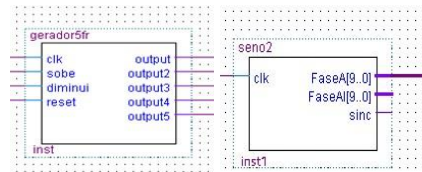

Fig. 4. Bloc "Grador" responsible for operating frequencies.

The 'Sine' block, illustrated in Figure 04, receives the signals from the generator at its input and is responsible for calculating the corresponding sinusoid for each adopted operating frequency. This includes considering the angular phase shift between the three phases of the motor and between the generated harmonics. Its structure includes reference values for the sinusoidal wave for each half-cycle and a memory to store this information.

The 'Attenuator' block, figure 5, is tasked with reducing the amplitude of each harmonic to adjust its influence. These harmonics will be individually summed and used to counteract the harmonics found in the motor's ripple torque signal during its operation. Their values will be manually defined within five stages but can also be controlled through a closed-loop system, utilizing resources such as machine learning or neural networks to determine how much attenuation is needed, at what time, and for which harmonic, given the motor's operating regime, which can be dynamic.
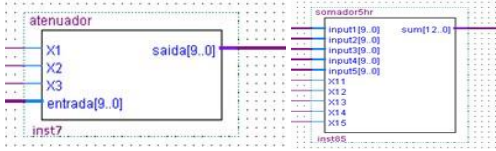
Fig. 5. Attenuator block responsible for attenuating the amplitudes of the harmonics.

The 'Adder' block, figure 5, is responsible for summing the fundamental signal and the harmonics for each phase. The generator's architecture was designed to allow the decision of which harmonic to inject and when to be made manually during motor operation. The injection or omission of each harmonic can be done autonomously, depending on the motor's operating regime and the predefined conditions set by the user.

The 'PWM' block, figure 6, the last block of the signal generator, is responsible for generating the PWM signal that will power the load, or power circuit, and interface with the reluctance motor. Its operation involves comparing the signal at its input with the defined sampling clock, based on the FPGA clock. The sampling frequency can be defined, affecting the harmonic content and resolution of the output signal from the generator.
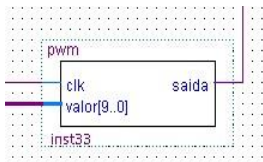
Fig. 6. Block 'PWM' responsible for generating the output signal

The expected signal at the output of the inverter block filter can be calculated according to the truncated Fourier series, witch represent a periodic function as a sum of sine allowing complex periodic waveforms to be analyzed and synthesized (1), as follows [7]:

(1) $A(f) = a1sin(f) + a2sin(2f) + a3sin(3f) + a4sin(4f) + a5sin(5f)$

Equation (1) describes the Fourier function for five elements, where A is the signal, a1, a2, a3, a4, and a5 are the amplitudes of each harmonic, and f is their respective frequency. The graph of the function, considering a1=1, a2=1/8, a3=1/6, a4=1/4, and a5=1/2, is as follows bellow in figure 7:
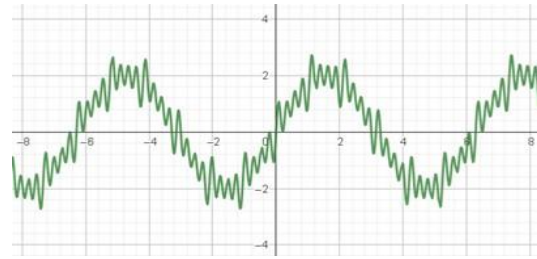
Fig. 7. The function graph calculated in GeoGebra.

The observed signal aims to nullify the ripple found in the torque and working current of the motor.

V. TESTS AND RESULTS

After assembling and simulating the waveform shapes of the signal generator through Quartus, the definition of input and output pins of the processor and the FPGA I/O outputs, which deliver a 3.3V analog signal, was carried out. The outputs were connected to an RC circuit composed of a 680Ω resistor and a 20nF capacitor, in a low-pass configuration, with a cutoff frequency of approximately 10kHz, as per equation 02, in order to observe the sinusoidal signal at the board's output, generated by the PWM pulses [7].

Equation employed for computing the low-pass filter, comprising a capacitor C and a resistor R (2), where in this case it will be used to allow us to observe the composition of the sine wave and the harmonics generated at the PWM output.

(2) $fc = 1/(2*\pi*R*C)$, (Rashid,1999)

We can observe in figure 8 the bench test setup of the project.

Fig. 8. Test setup, consisting of the oscilloscope, laptop, FPGA, and RC load

The sequence adopted for analyzing the output signal generated by the FPGA consists of first validating the pulse train generated by the PWM, the output block of the signal generator. Subsequently, the fundamental signal, which can vary from 50Hz to 1kHz, was analyzed, where each harmonic was individually added, and its waveform could be observed on the oscilloscope screen.

Finally, all combined signals were injected into the FPGA output, where the fundamental frequency and its 6th, 12th, 18th, and 24th harmonics could be observed, in a simulation scenario where the purpose of this composition is to compensate for the torque ripple generated by the reluctance motor.

The sinusoidal voltage signal can be observed in Figure 9, across the RC load.
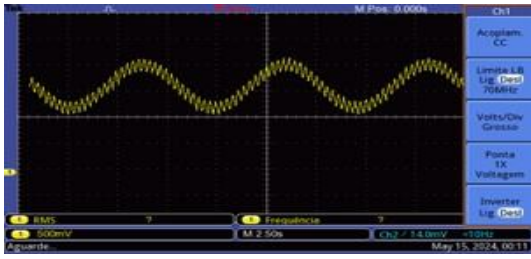
Fig. 9. Analysis of the fundamental frequency

We can notice a small ripple in the observed signal, resulting from the switching frequency of the signal generator, which could be eliminated with a better adjustment of the frequency of the configured RC (Low Pass) filter or possibly by adopting an inductive component to improve its performance [7].

After supplying the RC load with solely the fundamental frequency of the generator operation, we proceeded to introduce the harmonics, figure 10. A notable transformation in the waveform became apparent, wherein we observed cycles of the added harmonic within each sinusoidal half-cycle. This observation underscores the significance of the angular phase shift of these signals, as it defines their position within the waveform, thus playing a crucial role in shaping the composition of the final signal
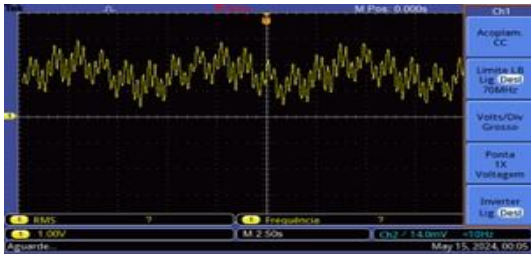

Fig. 10. Analysis of the fundamental frequency with its 24th harmonic

Finally, as we can observe in Figure 11, we enabled the sum of all harmonics to the fundamental signal, in a scenario where we would have the injection of all harmonics to combat torque ripple. At this point, we can notice a complex composition of signals distributed in the fundamental sine wave. Its angular phase shift and amplitude are crucial to ensure the quality of the output signal. This level of complexity requires high switching frequency values in the PWM block.
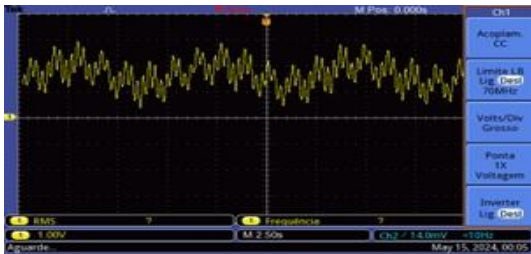

Fig. 11. Analysis of the signal with the fundamental frequency and all harmonics summed

During the testing phase, we varied the frequency of the fundamental signal from 50Hz to 1kHz. We summed each of the harmonics for different frequency values and varied their amplitude to test and verify the operation of the generator, as well as the effectiveness of the chosen PWM modulation switching frequency.

Appreciating the work "C. Lai, G. Feng, K. Lakshmi Varaha Iyer, K. Mukherjee, and N. C. Kar, 'Genetic Algorithm-Based Current Optimization for Torque Ripple Reduction of Interior PMSMs,' IEEE Trans Ind Appl, vol. 53, no. 5, pp. 4493–4503, Sep. 2017, doi: 10.1109/TIA.2017.2704063" as one of the main references for this study, we observed improved signal quality after implementing the technique, adding harmonics to suppress torque ripple.

VI. CONCLUSIONS

The main objective of the work is to create a signal generator for controlling a synchronous reluctance motor by adding harmonic components to its output signal, aiming to nullify the torque ripple generated mainly by the interaction of the stator magnetic flux and its interaction with the rotor's anisotropic geometry. The results obtained during the practical simulation confirm that the generator meets expectations.

As possible improvements and continuation of the study, we can vary the PWM switching frequency according to the motor's operating frequency, and also employ closed-loop control techniques to decide which harmonics to inject into the signal and their amplitude dynamically, considering machine learning, AI, among other resources. It would also be viable to map the motor's operating scenarios and store the working forms in memory, making 'work maps' available with instructions based on the learning acquired during data collection of these motors.

REFERENCES

[1] ABVE, "Eletrificados crescem 145% no trimestre," https://abve.org.br/eletrificados-crescem-145-no-trimestre-e-tem-segundo-melhor-mes-da-historia/.

[2] EPE, "BALANÇO ENERGÉTICO NACIONAL 2023," 2023. [Online]. Available: http://www.epe.gov.br

[3] S. D. Umans, *Maquinas Eletricas*, 7° Edition., vol. 7. 2014.

[4] C. Lai, G. Feng, K. Lakshmi Varaha Iyer, K. Mukherjee, and N. C. Kar, "Genetic Algorithm-Based Current Optimization for Torque Ripple Reduction of Interior PMSMs," *IEEE Trans Ind Appl*, vol. 53, no. 5, pp. 4493–4503, Sep. 2017, doi: 10.1109/TIA.2017.2704063.

[5] H. Salvador and M. Nunes, "Gerador se sinais digitais trifásicos com saída PWM," 2023.

[6] D. Emanuel *et al.*, "Motor síncrono de relutância para sistemas de tração de veículos elétricos," Coimbra, 2015. Accessed: Apr. 10, 2024. [Online]. Available: https://hdl.handle.net/10316/40460

[7] M. H. Rashid, *Eletrônica de Potência*. Makron Books, 1999.

[8] Terasic, "DE2_115_User_manual." 2017.

[9] Intel, "Intel ® Quartus ® Prime Standard Edition User Guides-Combined." 2019. Accessed: Apr. 09, 2024. [Online]. Available: https://www.intel.com/content/www/us/en/support/programmable/support-resources/design-software/user-guides.html